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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,028	11/26/2003	Timothy L. Blankenship	08211/0200253-US0/P05742	7271

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 08/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,028	BLANKENSHIP ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. The term "a telescopic cascode arrangement" in claim 1 and 20 are a relative term which renders the claim indefinite. The term "cascade transistor or a telescopic cascade arrangement" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. There is no teaching the cascode arrangement in the specification, furthermore, from figure 2 the cascode arrangement is just a PMOS transistor (M1) connected in series with NMOS transistors (M0), and a gate of M1 does not connected in conjunction with a source of transistor M8 instead to the drain of M8.

Claims 2-10, and 22 are rejected as dependent on claim 1 and 20.

3. Claim 22 recites the limitation "the second transistor" in the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Prodanov (6,693,469).

Prodanov shows:

1. A circuit (Fig. 4) comprising:

a first transistor (N5);

a second transistor (P5) that is arranged to operate as a cascode transistor in cooperation with the first transistor, as a telescopic cascade arrangement (P5 and N5 connected in series); and

a keeper switch circuit (P4) including three terminals that are respectively coupled to a gate, a drain, and a source of the second transistor.

2. The circuit of Claim 1, wherein the second transistor is configured to receive a first cascode bias voltage (Vmax) at the gate of the second transistor, and wherein the first cascode bias voltage is suitable for biasing a cascode transistor.

3. The circuit of Claim 1, wherein the keeper switch circuit is configured to influence a resistance between the source and the gate of the second transistor in response to a control signal (202).

4. The circuit of Claim 1, wherein the keeper switch circuit is configured to:

receive a control signal (g) at the drain of the second transistor; and

couple the source of the second transistor to the gate of the second transistor if the control signal corresponds to a first logic level (0 or LOW level).

5. The circuit of Claim 4, wherein the keeper switch circuit is further configured to isolate the source of the second transistor from the gate of the second transistor if the control signal corresponds to a second logic level (1 or HIGH level).

6. The circuit of Claim 1, wherein the keeper switch circuit comprises a keeper transistor including:

a gate that is coupled to the drain of the second transistor (P5 and N5);

a source that is coupled to one of a group consisting the source of the second transistor; and a drain that is coupled to the gate of the second transistor.

7. The circuit of Claim 6, wherein the second transistor is one of an n-type transistor or a p-type transistor, and the keeper transistor is the one of the n-type transistor or the p-type transistor.

8. The circuit of Claim 6, wherein the second transistor is one of an n-type transistor or the p-type transistor, and the keeper transistor is the other of the n-type transistor or the p-type transistor.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 9-10 are rejected under 35 U.S.C 102b as being anticipated by Annema et al (6,320414).

1. A circuit (Fig. 21) comprising:

a first transistor (PT2);

a second transistor (Tb6) that is arranged to operate as a cascode transistor in cooperation with the first transistor, as a telescopic cascade arrangement (connected in series); and

a keeper switch circuit (Tb5) including three terminals that are respectively coupled to a gate, a drain, and a source of the second transistor.

9. The circuit of Claim 1, further comprising: a third transistor (T*2); a fourth transistor (Tb*6) that is arranged to operate as a cascode transistor in cooperation with the third transistor; and another keeper switch circuit (Tb*5) including three terminals that are respectively coupled to a gate, a drain, and a source of the fourth transistor.

10. The circuit of Claim 9, wherein the other keeper switch circuit comprises a fifth transistor (NMOS transistor) including:

a gate that is coupled to the drain of the fourth transistor (a gate of Tb*5 connected to a drain of Tb*6), a source that is coupled to one of the source of the fourth transistor, and a drain that is coupled to the other the gate of the second transistor.

The limitations of claim 20 is rejected as above claims.

Allowable Subject Matter

3. Claims 11-19 are allowed.

4. The following is an examiner's statement of reasons for allowance: with respect to claim 11, in addition to other limitation in the claim, the prior art fails to teach or disclose the applicant's invention as claimed, particularly the feature describing the

connection of a second transistor, a fourth transistor, a first keeper switch circuit, and a second keeper switch circuit.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

5. Applicant's arguments filed 6/3/05 have been fully considered but they are not persuasive. Applicant defined the term cascode as "the term cascode may refer to the combination of common source transistor and the common-gate transistor, or may refer solely to a common gate transistor when used in conjunction with a common source transistor". Applicant's figure 2 shows a PMOS transistor (M1) as cascode transistor that have its gate connected to a drain of the keeper transistor (PMOS-M8). This feature are shows in Prodanov's reference and Annema's reference, furthermore the source of the second transistor and source of keeper transistor are coupled together as Applicant's claimed.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

8/11/05

ANH Q. TRAN
PRIMARY EXAMINER